A 95-GHz InP HEMT MMIC Amplifier with 427-mW Power Output

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***Abstract*— We have established a state-of-the-art InGaAs-InAlAs-InP HEMT MMIC fabrication process for millimeter-wave high-power applications. A two-stage monolithic microwave integrated circuit (MMIC) power amplifier with 0.15-μm gate length and 1.28-mm output periphery fabricated using this process has demonstrated an output power of 427 mW with 19% power-added efficiency at 95 GHz. To our knowledge, this is the highest output power ever reported at this frequency for any solid-state MMIC amplifier.**

I. Introduction

InP-BASED InAlAs-InGaAs HEMT's have demonstrated the highest cutoff frequency and lowest noise figure for any three-terminal solid-state devices [1], [2] due to their enhanced carrier confinement and superior transport properties. Very high gain InP HEMT MMIC LNA's have been realized at frequencies as high as 140–155 GHz [1], [3]. Because of its high gain, InP HEMT has also demonstrated excellent power-added efficiency (PAE) at millimeter-wave frequencies [4], [5]. The superior frequency response, noise figure, gain and efficiency makes InP HEMT's very suitable for millimeter- and submillimeter-wave applications. In this letter, we report the fabrication and world-record power performance of a 0.15-μm gate high-power InP HEMT MMIC amplifier fabricated using a high-yield monolithic microwave integrated circuit (MMIC) process.

II. Device and MMIC Process

The MMIC amplifier was fabricated on TRW's baseline InP power HEMT material profile grown on 3-in semi-insulating InP substrates. The structure consists of, from top to bottom, a depleted thin InGaAs cap layer, an undoped InAlAs Schottky barrier layer, a Si planar doping layer, an InAlAs spacer, an InGaAs channel layer, a bottom InAlAs spacer, a thin heavily doped InAlAs layer, and a thick InAlAs buffer. In the past few years, we have improved the material structure, delta doping density, ohmic contact layer, substrate thickness, compact device layout [4], and gate recess etch process [6] to optimize the millimeter-wave power performance.

Our 2-mil 0.15-μm gate high-power InP HEMT MMIC fabrication process is almost identical to that for our 3-mil 0.1-μm gate InP HEMT LNA process [3]. The devices are isolated using a combination of wet etch and boron implantation processes which provide better than 10 MΩ/square resistance. Source and drain ohmic contacts with Ni//Au-Ge/Ag/Au metals alloyed at 410°C using rapid thermal annealing provide very low contact resistance of 0.15 Ω-mm and source resistance of 0.2 Ω-mm. The 0.15-μm gate stripes are fabricated with a bilayered MPPA/PMMA-MAA resist profile for metal lift-off and metallization. The devices are gate recess etched to a predetermined current level which gives the best power and gain combination [6]. Typical peak transconductance, maximum channel current, and off-state drain-source breakdown voltage are 750, 650 mA/mm, and 7 V, respectively. The devices are passivated with 750-Å SiN deposited using PECVD. For the passive components, we perform precision NiCr resistor with a target resistance of 100 Ω/square and SiN MIM capacitors with a target sheet resistance of 300 pF/mm^2. After front side processing, the wafers are lapped and polished to 50-μm (2 mil) thickness. Then ground via holes are wet-chemical etched and 5-μm Au is plated on the backside of the wafers to complete the MMIC processing. We use 50-μm-thin substrates, which allows us to reduce the size of the via holes and place them closer to the source. This not only lowers parasitic source inductance, but also offers improved thermal conductivity.

III. MMIC Power Amplifier Performance

Using this production process we have fabricated and characterized a two-stage MMIC power amplifier which has a total gate periphery of 1.28 mm in the output stage. Shown in Fig. 1 is the photograph of this power amplifier. The chip size is 1.45 mm $\times$ 2.45 mm. We derived the output matching impedance of the amplifier based on a load line approach. Rigorous design and analysis methodology, including accurate device modeling and full-wave electromagnetic (EM) simulation of passive structures ensured the optimization of power, gain, and bandwidth.

We have carried out on-wafer pulse power test and in-fixture cw test to evaluate the amplifier performance. Fig. 2(a) shows output power versus input power curves measured on wafer at 95 GHz. The circuits were biased at a V_{gs} of 0 V. The drain voltage (2.5 V) and radio frequency (RF) input were pulsed simultaneously with a pulse width of 40 μs and a duty cycle of 10%. The tightly grouped $P_{\rm in}$-$P_{\rm out}$ curves indicate the uniformity of the devices. Fig. 2(b) shows the power performance of the amplifier measured in fixture at 95 GHz. When biased at $V_{ds} = 3$ V and $V_{gs} = 0$ V, the amplifier

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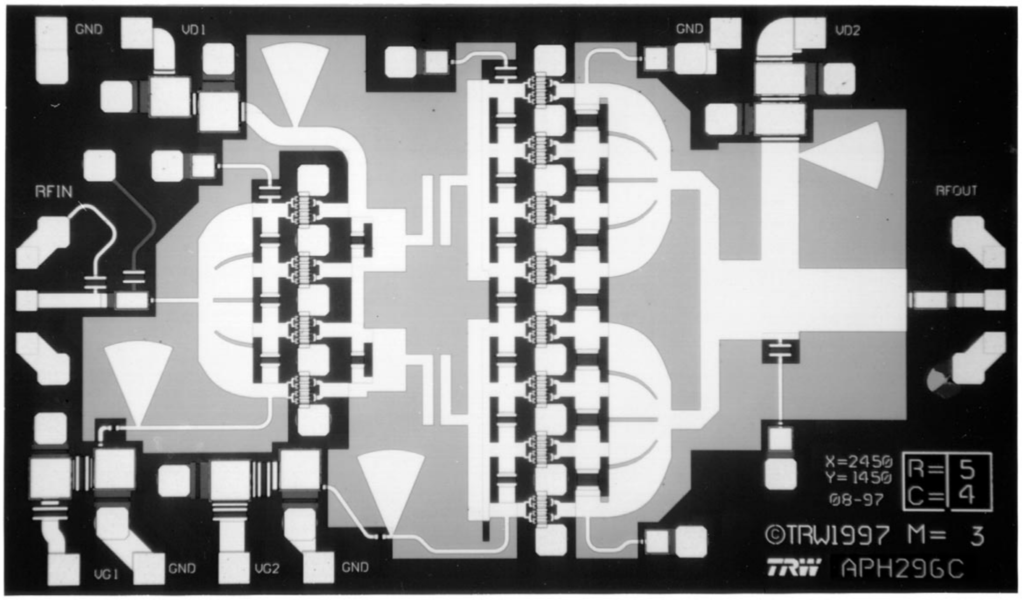
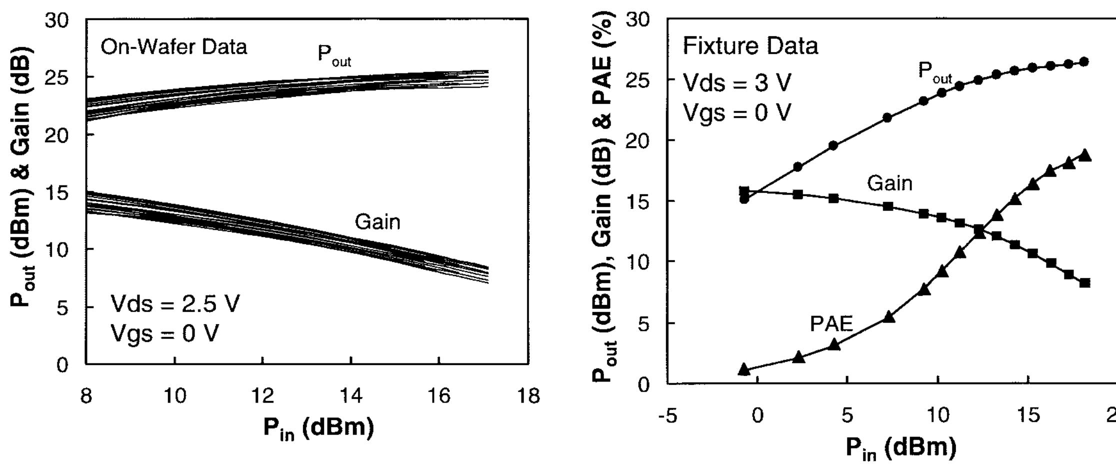


Fig. 1. Photograph of a two-stage 0.15-μm gate InP HEMT MMIC power amplifier.



(a) (b)

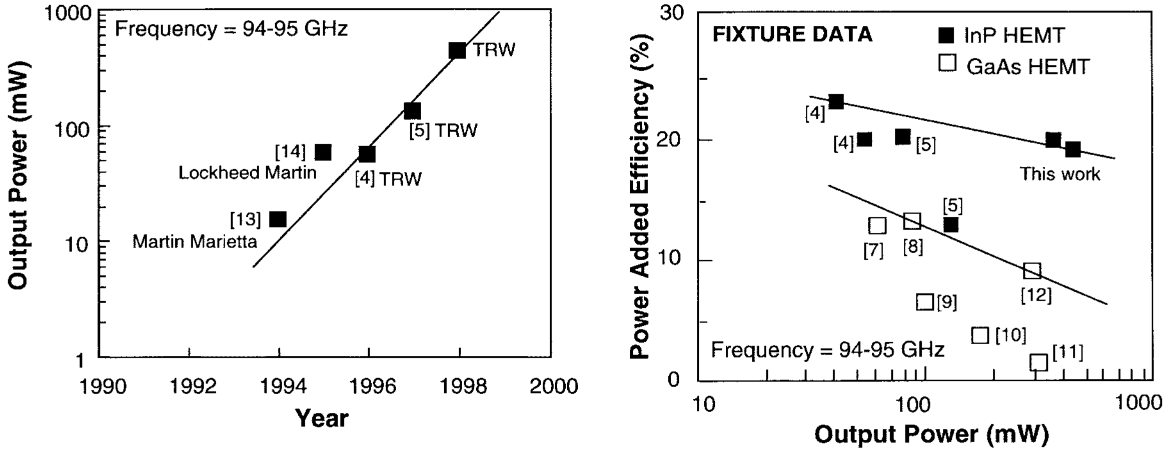
Fig. 2. 95-GHz power performance of two-stage 0.15-μm gate InP HEMT MMIC power amplifiers measured (a) on wafer under pulse power conditions and (b) in fixture under cw conditions.

delivered an output power of 427 mW with 19% PAE and 8.2-dB associated gain. When biased for best efficiency, the amplifier demonstrated a PAE of 20% at an output power of 400 mW. The associated gain was 8.8 dB. These data have been corrected for the waveguide-to-microstrip end-to-end insertion loss which was measured to be 1.5 dB. These results far exceeded our previous record of 130 mW with 13% PAE measured at 94 GHz [5]. To our knowledge, this is the highest output power ever reported at this frequency for any solid-state MMIC amplifiers. We attribute this improvement to the stable fabrication process that allows for accurate modeling of very high performance devices and the load line design approach that fully explores the device capability.

Fig. 3(a) shows the reported best 94–95-GHz power output measured from a single InP HEMT chip as a function of year. In less than four years we have achieved an output power almost 30 times higher than the first published result [13]. Fig. 3(b) compares the power and efficiency performance of various InP HEMT and GaAs HEMT MMIC power amplifiers measured in fixture at W-band. InP-based InAlAs-InGaAs HEMT's clearly outperformed their GaAs-based counterparts in terms of PAE as well as total power output. At similar output powers greater than 400 mW, InP HEMT power amplifiers exhibited twice the PAE compared to a GaAs HEMT power amplifier. This achievement enables the development of next-generation communication and electronic warfare systems which require high-power and high-efficiency millimeter-wave power amplifiers and arrays.

IV. Conclusions

We have developed a two-stage InP HEMT MMIC power amplifier with 0.15-μm gate length and 1.28-mm output periphery fabricated using our state-of-the-art InGaAs-InAlAs-InP HEMT MMIC fabrication process. The amplifier demon-



(a) (b)

Fig. 3. (a) Progress in InP HEMT power performance at 94–95 GHz. (b) Comparison of PAE versus output power for InP- and GaAs-based HEMT MMIC amplifiers measured at W-band.

strated an output power of 427 mW with 19% power-added efficiency at 95 GHz as measured in fixture. The result outperformed any solid-state MMIC power amplifiers in terms of PAE as well as total power output at this frequency. This clearly suggests that InP-based HEMT's are the best candidate for millimeter-wave high power and high-efficiency applications at W-band.

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